REMARKS

In accordance with the foregoing, claims 7, 18, 27, and 36 are amended herein to correct an informality. No new matter is being presented, and approval and entry are respectfully requested.

Claims 1-41 are pending and under consideration. Reconsideration is requested.

Item 4: Objection To Claims 7, 18, 27, and 36

In item 4 of the Office Action, the Examiner objects to claims 7, 18, 27, and 36. (Action at pages 3-4). The Examiner asserts:

> Claim 7, Lines 3-4, "hardware resource allocated by said resource request in said requesting a resource" appears to be incorrect and it appears that it should be " hardware resource allocated by said resource manager in said allocating a resource.

(See, Action at page 3). In support of the objection, the Examiner makes similar assertions regarding claims 18, 27, and 36.

Claims 7, 18, 27, and 36 are amended in accordance with the Examiner's suggestions and withdrawal of the objection is requested.

Item 6: Rejection of Claims 1-41 under 35 U.S.C. §112, first paragraph

The Examiner rejects claims 1-41 under 35 USC §112, first: paragraph as containing subject matter that was not described in the specification at the time the application was filed.

The Amendment filed October 10, 2006 ("previous Amendment") amended independent claim 1, for example, to recite a method including "requesting a resource in which a thread manager . . . , makes a request for information about a hardware resource relating to a hardware resource needed for execution of each of threads representative of a series of functions required until the operation of said logical unit reaches completion according to a design specification of said logical unit, to a resource manager which manages said information about the hardware resource; allocating a resource in which said resource manager allocates said information about a hardware resource meeting said request . . . while dynamically allocating information about a hardware resource-relating to necessary hardware resources . . . ." (Emphasis added). Independent claims 12-14 and 41 were similarly amended. Dependent claims 4-5, 7-10, 15-16, 18-21, 24-25, 27-30, 33-34, and 36-39 were amended to correspond to respective amended parent claims.

In the previous Amendment, Applicants submitted that support is found, for example, in paragraphs [0050], [0051], [0054], [0055], and [0057]-[0060] of the Substitute Specification.

However, in rejecting claim 1 in the current Office Action, for example, the Examiner merely asserts that such a recitation about "information about a hardware resource" is:

> [N]ew material added in the amendment and not found in the original specification. The applicants are required to show where in the specification information about a hardware resource is described.

(Action at page 5). The Examiner makes similar assertions regarding other claims. (Action at pages 4-20).

However, as set forth in MPEP §2164.04 Burden on the Examiner Under *>the< Enablement Requirement:.

> In order to make a rejection, the examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. . . . A specification disclosure which contains a teaching of the manner and process of making and using an invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented must be taken as being in compliance with the enablement requirement of 35 U.S.C. 112, first paragraph, unless there is a reason to doubt the objective truth of the statements contained therein which must be relied on for enabling support. . . . As stated by the court, "it is incumbent upon the Patent Office, whenever a rejection on this basis is made, to explain why it doubts the truth or accuracy of any statement in a supporting disclosure and to back up assertions of its own with acceptable evidence or reasoning which is inconsistent with the contested statement. Otherwise, there would be no need for the applicant to go to the trouble and expense of supporting his presumptively accurate disclosure." . . . the minimal requirement is for the examiner to give reasons for the uncertainty of the enablement. This standard is applicable even when there is no evidence in the record of operability without undue experimentation beyond the disclosed embodiments.

Applicants submit the Examiner's assertion is not backed up with, as required, "assertions of its own with acceptable evidence or reasoning." As set forth in MPEP §706.03(c) for Rejections Under 35 U.S.C. 112, First Paragraph:

> The explanation should include any questions the examiner may have asked which were not satisfactorily resolved and consequently raise doubt as to enablement.

Applicants submit that the current Office Action is incomplete, since the Examiner has not provided required support for the rejection that raise doubt as to enablement. Thus, if the rejection is not withdrawn, Applicants request another non-final Office Action be issued with complete support by the Examiner and with the due date accordingly reset.

Applicants submit that claims 1-41 are supported by the specification and comply with 35 U.S.C. §112, first paragraph, and that all of the claim language is supported, including, the recited language, "information about a hardware resource."

For example, as disclosed in the specification:

> [T]he resource 14 signifies information about a hardware resource. For example, each of processors, ASICs (Application Specific Integrated Circuits), operation units and other units is defined as resource data.

(Emphasis added, See, for example, page 22, lines 8-11 of the specification, paragraph [0052] of the Substitute Specification).

That is, as disclosed in page 22, lines 8-11 of the specification, "resource 14" signifies "information about a hardware resource," and according to an example embodiment of the present invention each subsequent disclosure of "resource 14" signifies information about a hardware resource. For example, as disclosed in the specification:

> In addition, the thread manager 11 fetches the execution waiting thread 13 from the execution waiting queue 18 after the input queue 17 is void, and if that thread 13 is in the non-initiation condition, executes and sets it into an "execution condition" (step S7). When entering the "execution condition", the thread 13 makes a request to the resource manager 12 for securing the resource 14 needed for the first "method" (for example, issues a resource request 19 for the resource "B" of the resources "A" to "C"; step S8, resource request step). This resource request 19 is added through the thread manager 11 to the resource request queue 20. Moreover, the thread 13 which has issued this resource request 19 is added to the last of the execution waiting queue 18.

(Emphasis added, See, for example, page 25, lines 13-26 of the specification, paragraph [0065] of the Substitute Specification).

That is, as understood by one of ordinary skill in the art as discussed in the specification, disclosed in page 22, lines 8-11 of the specification resource 14 signifies information about a hardware resource. and each subsequent disclosure of resource 14 signifies information about a hardware resource. As discussed in the previous Amendment, further support is found, for example, in paragraphs [0050], [0051], [0054], [0055], and [0057]-[0060] of the Substitute Specification.

Summary

Applicants submit that claims 1-41 are supported by the specification and comply with 35 U.S.C. §112, first paragraph and request the rejection be withdrawn.

Further, since the Examiner has not provided required support for the rejection that raise doubt as to enablement, in the event the rejection is not withdrawn, Applicants request another non-final Office Action with the due date accordingly reset.

Item 7: Claim Interpretation

In item 7 of the Office Action, the Examiner asserts that since in the Summary of the Invention the specification discloses an example embodiment including "a resource requesting

step in which a thread manager, which controls threads each forming an execution unit of a program, makes a request for hardware resource. . . a resource allocating step in which said resource manager allocates the hardware resource . . .resource manager dynamically allocates a needed hardware resource whenever the thread is executed," that:

> Therefore, the Examiner has interpreted all references to "information about hardware resource" as "hardware resource". These interpretations are used in the following art rejections.

(Emphasis added, see, page 21).

Applicants submit that the current recitations of claims 1-41 are supported by the specification and the Examiner's interpretation of "information about hardware resource" as "hardware resource" is not correct.

Item 10: Rejection of claims 1-7, 10-18, 21-27, 30-36 and 39-41 under 35 U.S.C. §103(a) as being unpatentable over Emer et al. (U.S.Patent 6,493,741) in view of Stamm et al. (U.S. Patent 6,711,616)

Item 11: Rejection of claims 8, 19, 28 and 37 under 35 U.S.C. §103(a) as being unpatentable over Emer in view of Stamm and further in view of Chrysos et al. (U.S. Patent 6,549,930)

In item 10 of the Office Action, the Examiner rejects claims 1-7, 10-13, 21-27, 30-36, and 39-41 under 35 U.S.C. §103(a) as being unpatentable over Emer in view of Stamm and in item 11 of the Office Action, the Examiner rejects claims 8, 19, 28, and 37 as being unpatentable over Emer in view of Stamm and further in view of Chyrsos. The rejections are traversed.

Applicants submit that none of the art relied on by the Examiner, even in *arguendo* combination, teach features recited by each of the independent claims. Claim 1, for example, recites a method of simulating an operation of a logical unit, including:

(1) "requesting a resource in which a thread manager makes a request for information about a hardware resource relating to a hardware resource needed for execution of each of threads representative of a series of functions required until the operation of said logical unit reaches completion according to a design specification of said logical unit, to a resource manager which manages said information about the hardware resource" and

(2) "allocating a resource in which said resource manager allocates said information about a hardware resource meeting said request to said thread in accordance with a rule prescribed in advance," and

(3) "controlling a thread in which said thread manager controls an execution state of said thread in accordance with a result of the allocation made by said resource manager,"

(4) "said thread manager and said resource manager executing said:

(4) a) "requesting, allocating, and controlling repeatedly in cooperation with each other until the execution of said thread reaches completion while"

(4) b) "dynamically allocating information about a hardware resource relating to necessary hardware resources to the thread by said resource manager every time the generated thread is executed simulating the operation of said logical unit to be conducted up to the completion."

In particular, none of the cited art teach such a "requesting a resource in which a thread manager, which controls threads each forming an execution unit of a program, makes a request for information about a hardware resource (emphasis added)," as recited by claim 1, for example.

Further, none of the cited art, alone or in combination, teach "allocating information about a hardware resource relating to necessary hardware resources to the thread by said resource manager every time the generated thread is executed simulating the operation of said logical unit to be conducted up to the completion (emphasis added)," as recited by claim 1, for example.

That is, none of the cited art teach a simulation using information relating to necessary hardware resources, as recited in each of the independent claims.

The Examiner asserts that Emer col. 2, lines 3-6 teaches "requesting a resource in which a thread manager makes a request for information about a hardware resource relating to a hardware resource needed for execution of each of threads . . . to a resource manager which manages said information about the hardware resource," as recited by claim 1, for example. (Action at page 23). However, Emer merely teaches:

> Sequence (c) 6 corresponds to a simultaneous multithreaded architecture and shows how each cycle in an SMT processor selects instructions for execution from all threads. It exploits instruction-level parallelism by selecting instructions from any thread that can potentially issue. The processor then dynamically schedules machine resources among the instructions, providing the greatest chance for the highest hardware utilization. If one thread has high instruction-level parallelism, that parallelism can be satisfied; if multiple threads each have low instruction-level parallelism, they can be executed simultaneously to compensate. In this way, SMT can recover issue slots lost to both horizontal and vertical waste.

(See, for example, col. 1, line 66 - col. 2. line 10)

However, claim 1 recites, for example, a method "allocating information about a hardware resource relating to necessary hardware resources to the thread by said resource manager every time the generated thread is executed simulating the operation of said logical unit to be conducted up to the completion (emphasis added)."

The Action concedes that Emer does not teach "allocating a resource in which the resource manager allocates the information about a hardware resource." (Action at page 23). However, the Examiner asserts Stamm et al. teaches "allocating a resource in which the resource manager allocates the information about a hardware resource." (Action at page 25).

Applicants submit that even an *arguendo* combination of the art relied on by the Examiner does not teach "allocating information about a hardware resource relating to necessary hardware resources to the thread by said resource manager every time the generated thread is executed simulating the operation of said logical unit, as recited by claim 1." By contrast, Stamm teaches:

> When server 20 receives a work request from a client, server 20 finds the subtask with resource requirements best matching the available resources of the requesting client. In another embodiment, the tasks are further categorized, and each category is allotted a selected portion of the total of the available resources. The selection of a subtask by server 20 is partially based on the portions of the total available computational resources already allocated to the various categories of tasks, as further illustrated and explained in FIG. 5.

(See, for example, col. 3, lines 10-20).

That is, Stamm merely teaches a distribution of tasks. In rejecting dependent claims 8, 19, 28 and 37 the Examiner relies on Chryos as teaching a monitoring of a number of resource requests.

Applicants submit that the disclosure in Chyros does overcome the deficiencies in the art not teaching features recited by each of the independent claims, as discussed above. By contrast, Chryos merely teaches:

> Resource utilizations of each of the plurality of threads is measured while the plurality of threads are concurrently executing in the multithreaded processor. Each of the plurality of threads is scheduled according to the measured resource utilizations using a thread scheduler.

(See, for example, col. 7, lines 45-50).

Applicant further submits that this traversal meets the Consideration of Applicant's Rebuttal Evidence Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme Court Decision in *KSR* International Co. v. Teleflex Inc. of October 3, 2007.

Summary

Since features recited by each of the independent claims and respective dependent claims are not taught by the art relied on by the Examiner even in combination, the rejection should be withdrawn and claims 1-41 allowed.

Conclusion

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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